IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellants:	SOUK, Jun-Hyung; LEE, Jeong-Young; YOON, Jong-Soo; CHOI, Kwon-Young; and BAEK, Bum-Ki		
Assignee:	Samsung Electronics Co., Ltd.		
Title:	THIN FILM TRANSISTOR ARRAY PANEL AND MANUFACTURING METHOD THEREOF		
Application No.:	10/759,389	Filing Date:	01/16/04
Examiner:	Ton, Minh Toan T.	Group Art Unit:	2871
Docket No.:	AB-1351 US	Confirmation No.:	6707

San Jose, California
August 3, 2006

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

APPEAL BRIEF UNDER 37 CFR § 41.37

Dear Sir:

Appellant submits this Appeal Brief in support of the Notice of Appeal filed in this case on April 26, 2006. Pursuant to the Notice of Panel Decision from Pre-Appeal Brief Review, the deadline for filing this Appeal Brief is July 7, 2006 (one month from the mailing of the Notice). Accompanying this Appeal Brief is a Petition for a One-Month Extension of Time pursuant to 37 C.F.R § 1.136, thereby extending the deadline for filing this Appeal Brief to August 7, 2006.

The accompanying transmittal letter authorizes the Commissioner for Patents to deduct from the undersigned Attorney's deposit account the required fees for filing this Appeal Brief and accompanying Extension of Time.

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I. REAL PARTY IN INTEREST

The real party in interest is Assignee SAMSUNG ELECTRONICS CO., LTD.

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II. RELATED APPEALS AND INTERFERENCES

There are no appeals or interferences known to Appellant, Appellant's legal representative, or the Assignee which will directly affect or be directly affected by or have a bearing on the decision by the Board of Patent Appeals in the pending appeal.

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III. STATUS OF CLAIMS

Claims 1-29 are pending in the application. Claims 6-14 are withdrawn from consideration. Claims 1-5 and 15-29 are rejected and appealed.

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IV. STATUS OF AMENDMENTS

On February 28, 2006, Appellant filed a Response to Final Office Action in which claims 1-14 and 20-24 were canceled, leaving claims 15-19 and 25-29 under consideration.

On March 16, 2006, the Examiner issued an Advisory Action which was silent as to the status of the proposed amendments filed in the Response to Final Office Action.

On June 7, 2006, a Notice of Panel Decision from Pre-Appeal Brief Review was issued. This Notice indicated that the panel has determined the status of the claims as follows: claims 1-5 and 15-29 rejected, and claims 6-14 withdrawn from consideration.

On August 2, 2006, Appellant filed an Amendment in which Appellant again requested cancellation of claims 1-14 and 20-24. No notice has been received regarding the status of this Amendment.

Appellant submits that because the amendment in the Response to Final Office Action filed on February 28, 2006, was limited to solely the cancellation of claims, this amendment should have been entered.

Alternatively, the Amendment filed on August 2, 2006 should be entered pursuant to MPEP § 1206 and 37 C.F.R § 41.33, because it, too, is limited solely to the cancellation of claims.

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V. SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 1 recites a thin film transistor array panel (panel 100 in FIG. 1, described in part on page 6, lines 7-10). The panel includes: a gate line (gate line 121 in FIGS. 2-3, described in part on page 6, line 22 to page 7, line 13) formed on an insulating substrate (insulating substrate 110 of FIG. 3, described in part on page 6, lines 22-23); a gate insulating layer (gate insulating layer 140 in FIG. 3, described in part on page 7, lines 14-15) on the gate line; a semiconductor layer (semiconductor stripes 151, described in part on page 7, lines 16-21) on the gate insulating layer; a data line (data lines 171 of FIGS. 2-3, described in part on page 7, line 30 to page 8, line 21) formed on the gate insulating layer and including a source electrode (source electrodes 173 of FIGS. 2-3, described in part on page 8, lines 2-8); a drain electrode (drain electrodes 175 of FIGS. 2-3, described in part on page 7, line 30 to page 8, line 21) formed at least in part on the semiconductor layer; a passivation layer (passivation layer 180 of FIG. 3, described in part on page 8, lines 31 to page 9, line 16) formed on the data line and the drain electrode and having a first contact hole (contact hole 185 of FIGS. 2-3, described in part on page 9, lines 5-16) exposing the drain electrode at least in part and a portion of the gate insulating layer; and a pixel electrode (pixel electrodes 191 of FIGS. 2-3, described in part on page 9, line 17 to page 10 line 8) formed on the passivation layer and contacting the drain electrode and the exposed portion of the gate insulating layer through the first contact hole, wherein the gate insulating layer separates the pixel electrode from the insulating substrate.

Independent claim 15 recites a thin film transistor array panel (panel 100 in FIG. 1, described in part on page 6, lines 7-10). The panel includes: a gate line (gate line 121 in FIGS. 2-3, described in part on page 6, line 22 to page 7, line 13) formed on an insulating substrate (insulating substrate 110 of FIG. 3, described in part on page 6, lines 22-23); a gate insulating layer (gate insulating layer 140 in FIG. 3, described in part on page 7, lines 14-15) on the gate line; a semiconductor layer (semiconductor stripes 151, described in part on page 7, lines 16-21) on the gate insulating layer; a data line (data lines 171 of FIGS. 2-3, described in part on page 7, line 30 to page 8, line 21) formed on the gate insulating layer and including

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a source electrode (source electrodes 173 of FIGS. 2-3, described in part on page 8, lines 2-8); a drain electrode (drain electrodes 175 of FIGS. 2-3, described in part on page 7, line 30 to page 8, line 21) formed at least in part on the semiconductor layer; a passivation layer (passivation layer 180 of FIG. 3, described in part on page 8, lines 31 to page 9, line 16) formed on the data line and the drain electrode and having a first contact hole (contact hole 185 of FIGS. 2-3, described in part on page 9, lines 5-16) exposing the drain electrode at least in part and a portion of an upper surface of the gate insulating layer; and a pixel electrode (pixel electrodes 191 of FIGS. 2-3, described in part on page 9, line 17 to page 10 line 8) formed on the passivation layer and contacting the drain electrode and the exposed portion of the gate insulating layer through the first contact hole.

Independent claim 20 recites a thin film transistor array panel (panel 100 in FIG. 1, described in part on page 6, lines 7-10). The panel includes: a gate line (gate line 121 in FIGS. 2-3, described in part on page 6, line 22 to page 7, line 13) formed on an insulating substrate (insulating substrate 110 of FIG. 3, described in part on page 6, lines 22-23); a gate insulating layer (gate insulating layer 140 in FIG. 3, described in part on page 7, lines 14-15) on the gate line; a semiconductor layer (semiconductor stripes 151, described in part on page 7, lines 16-21) on the gate insulating layer; a data line (data lines 171 of FIGS. 2-3, described in part on page 7, line 30 to page 8, line 21) formed on the gate insulating layer and including a source electrode (source electrodes 173 of FIGS. 2-3, described in part on page 8, lines 2-8); a drain electrode (drain electrodes 175 of FIGS. 2-3, described in part on page 7, line 30 to page 8, line 21) formed at least in part on the semiconductor layer; a passivation layer (passivation layer 180 of FIG. 3, described in part on page 8, lines 31 to page 9, line 16) formed on the data line and the drain electrode and having a first contact hole (contact hole 185 of FIGS. 2-3, described in part on page 9, lines 5-16), wherein a bottom of the contact hole is formed by a portion of an upper surface of the drain electrode and a portion of an upper surface of the passivation layer; and a pixel electrode (pixel electrodes 191 of FIGS. 2-3, described in part on page 9, line 17 to page 10 line 8) formed on the passivation layer and contacting the drain electrode and the exposed portion of the gate insulating layer through the first contact hole.

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Independent claim 25 recites a thin film transistor array panel (panel 100 in FIG. 1, described in part on page 6, lines 7-10). The panel includes: a gate line (gate line 121 in FIGS. 2-3, described in part on page 6, line 22 to page 7, line 13) formed on an insulating substrate (insulating substrate 110 of FIG. 3, described in part on page 6, lines 22-23); a gate insulating layer (gate insulating layer 140 in FIG. 3, described in part on page 7, lines 14-15) on the gate line; a semiconductor layer (semiconductor stripes 151, described in part on page 7, lines 16-21) on the gate insulating layer; a data line (data lines 171 of FIGS. 2-3, described in part on page 7, line 30 to page 8, line 21) formed on the gate insulating layer and including a source electrode (source electrodes 173 of FIGS. 2-3, described in part on page 8, lines 2-8); a drain electrode (drain electrodes 175 of FIGS. 2-3, described in part on page 7, line 30 to page 8, line 21) formed at least in part on the semiconductor layer; a passivation layer (passivation layer 180 of FIG. 3, described in part on page 8, lines 31 to page 9, line 16) formed on the data line and the drain electrode and having a first contact hole (contact hole 185 of FIGS. 2-3, described in part on page 9, lines 5-16) exposing the drain electrode at least in part and a portion of the gate insulating layer; and a pixel electrode (pixel electrodes 191 of FIGS. 2-3, described in part on page 9, line 17 to page 10 line 8) formed on the passivation layer and contacting the drain electrode and the exposed portion of the gate insulating layer through the first contact hole, wherein the pixel electrode contacts an upper surface of the gate insulating layer.

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VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether claims 1-14 and 20-24 have been canceled.

Whether claim 1 is unpatentable under 35 USC § 102(b) as being anticipated by U.S. Patent No. 6,414,730 ("Akamatsu").

Whether claims 2-5 and 15-29 are unpatentable under 35 U.S.C. § 103(a) over U.S. Patent No. 6,414,730 ("Akamatsu").

Whether claims 1-5 are unpatentable based on nonstatutory double patenting.

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VII. ARGUMENT

Whether claims 1-14 and 20-24 have been canceled.

As described above, Appellant has attempted to cancel claims 1-14 and 20-24 in a Response to Final Office Action filed on February 28, 2006, and in an Amendment filed on August 2, 2006. No notice has been received regarding the status of these attempted amendments.

Appellant submits that because the amendment in the February 28, 2006, Response to Final Office Action was limited to solely the cancellation of claims, this amendment should have been entered. Alternatively, the Amendment filed on August 2, 2006 should be entered pursuant to MPEP § 1206 and 37 C.F.R § 41.33, because it, too, is limited solely to the cancellation of claims.

Whether claim 1 is unpatentable under 35 USC § 102(b) as being anticipated by U.S. Patent No. 6,414,730 ("Akamatsu").

In the Final Office Action dated December 29, 2005, the Examiner rejected claim 1 as being anticipated by Akamatsu et al. (U.S. Pat. No. 6,414,730). As described above, claim 1 should be canceled, thereby making moot the Examiner's rejection under § 102.

Whether claims 2-5 and 15-29 are unpatentable under 35 U.S.C. § 103(a) over U.S. Patent No. 6,414,730 ("Akamatsu").

The Examiner has rejected claims 2-5 and 15-29 as being unpatentable over the Akamatsu reference as applied to claim 1. As described above, claims 2-5 and 20-24 should be canceled, thereby making moot the rejection of claims 2-5 and 20-24 under § 103. Accordingly, claims 15-19 and 25-29 should remain under consideration. In the Advisory Action, the Examiner states, in part:

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> The request for reconsideration has been considered but does NOT place the application in condition for allowance because: . . . the arguments are found not persuasive. Akamatsu discloses the device comprising the pixel electrode contacting an upper surface of the gate insulating layer (see at least Figure 2A) and a first contact hole exposing a portion of an upper surface of the gate insulating layer (also see at least Figure 2A). Thus, the final rejection stands.

Applicants respectfully traverse the Examiner's rejection. Claim 15 recites, in part:

> a passivation layer formed on the data line and the drain electrode and having a first contact hole exposing the drain electrode at least in part and a portion of an upper surface of the gate insulating layer; and
>
> a pixel electrode formed on the passivation layer and contacting the drain electrode and the exposed portion of the gate insulating layer through the first contact hole.
>
> (Emphasis added.)

Applicants submit that the Examiner has failed to provide any support for modifying the Akamatsu reference to provide a structure having "a first contact hole exposing the drain electrode at least in part and a portion of an upper surface of the gate insulating layer" and a pixel electrode contacting "the exposed portion of the gate insulating layer through the first contact hole", as recited in claim 15. Therefore, the Examiner has failed to establish a *prima facie* case of obviousness.

Contrary to the Examiner's assertion, Figure 2A of the Akamatsu reference fails to teach or suggest the claimed structure. As can be seen in Figure 2A, the through hole 87 does not expose an upper surface of the gate insulation film 53. Instead, Figure 2A shows that the through hole 87 exposes an upper surface of one end 59b of the drain extraction electrode 59. The pixel electrode 69 is connected to the drain extraction electrode 59 via the through hole 87. The Examiner has failed to provide any indication of how Figure 2A discloses the exposing a portion of the upper surface of the gate insulation layer.

Applicants respectfully request that the Board reverse the rejection under 35 U.S.C. § 103 of claim 15 and claims 16-19, which depend from claim 15, and allow the claims.

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Claim 25 recites, in part:

> a pixel electrode formed on the passivation layer and contacting the drain electrode and the exposed portion of the gate insulating layer through the first contact hole, wherein the pixel electrode contacts an upper surface of the gate insulating layer. (Emphasis added.)

As described above with respect to claim 15, the Examiner has failed to provide any support for how the Akamatsu reference discloses the claimed structure in which the pixel electrode contacts an upper surface of the gate insulating layer, as recited in claim 25. Therefore, the Examiner has failed to establish a *prima facie* case of obviousness and the Examiner's rejection is unsupported.

Applicants respectfully request that the Board reverse the rejection under 35 U.S.C. § 103 of claim 25 and claims 26-29, which depend from claim 25, and allow the claims.

Whether claims 1-5 are unpatentable based on nonstatutory double patenting.

Claims 1-5 have been rejected under the judicially-created doctrine of obviousness-type double patenting over claims of U.S. Publication No. 2005/0030440 to Lee et al. As described above, claims 1-5 should be canceled, thereby making moot the rejection of claims 1-5 for nonstatutory double patenting.

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CONCLUSION

For the foregoing reasons, Appellant respectfully submits that claims 1-14 and 20-24 be canceled and claims 15-19 and 25-29 be allowed.

If the Examiner or the Board have any questions regarding the above, they are respectfully requested to telephone the undersigned Attorney for Applicants at 408-392-9250.

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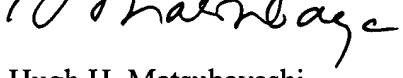
Respectfully submitted,



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CLAIMS APPENDIX A

Claims 1-29 are pending in the application. Claims 6-14 are withdrawn from consideration. Claims 1-5 and 15-29 are rejected and appealed.

Claim 1 (Previously presented): A thin film transistor array panel comprising:

a gate line formed on an insulating substrate;

a gate insulating layer on the gate line;

a semiconductor layer on the gate insulating layer;

a data line formed on the gate insulating layer and including a source electrode;

a drain electrode formed at least in part on the semiconductor layer;

a passivation layer formed on the data line and the drain electrode and having a first contact hole exposing the drain electrode at least in part and a portion of the gate insulating layer; and

a pixel electrode formed on the passivation layer and contacting the drain electrode and the exposed portion of the gate insulating layer through the first contact hole, wherein the gate insulating layer separates the pixel electrode from the insulating substrate.

Claim 2 (Previously presented): The thin film transistor array panel of claim 1, wherein at least one of the gate line, the data line, and the drain electrode comprises a lower film of Cr, Mo, or Mo alloy and an upper film of Al or Al alloy.

Claim 3 (Previously presented): The thin film transistor array panel of claim 1, wherein the gate insulating layer comprises silicon nitride and the passivation layer comprises silicon nitride.

Claim 4 (Previously presented): The thin film transistor array panel of claim 1, wherein the pixel electrode comprises IZO.

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Claim 5 (Previously presented): The thin film transistor array panel of claim 1, wherein the passivation layer has second and third contact holes exposing end portions of the

gate line and the data line, and the thin film transistor array panel further comprises contact assistants contacting the exposed end portions of the gate line and the data line.

Claim 6 (Withdrawn): A method of manufacturing a thin film transistor array panel, the method comprising:

forming a gate line on an insulating substrate;

forming a gate insulating layer;

forming a semiconductor layer;

forming a data conductive layer including a data line and a drain electrode;

depositing a passivation layer;

forming a photoresist including a first portion located on an end portion of the gate line, a second portion thicker than the first portion and located on the drain electrode, and a third portion thicker than the second portion;

exposing a portion of the passivation layer under the second portion of the photoresist and a portion of the gate insulating layer under the first portion of the photoresist by etching using the photoresist as an etch mask;

forming first and second contact holes exposing the drain electrode and the end portions of the gate line, respectively; and

forming a pixel electrode connected to the drain electrode through the first contact hole.

Claim 7 (Withdrawn): The method of claim 6, wherein the photoresist further comprises a fourth portion disposed on an end portion of the data line, and the method further comprises forming a third contact hole exposing the end portion of the data line.

Claim 8 (Withdrawn): The method of claim 6, wherein the exposure is performed by dry etching under a condition that etching ratios for the photoresist and the passivation layer are substantially the same.

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Claim 9 (Withdrawn): The method of claim 6, wherein the exposed portion of the gate line is thicker than the exposed portion of the passivation layer.

Claim 10 (Withdrawn): The method of claim 6, wherein the formation of the first and second contact holes is performed by dry etching under a condition that etching ratios for the gate insulating layer and the passivation layer are substantially the same.

Claim 11 (Withdrawn): The method of claim 6, wherein the gate line or the data line comprises a lower film of Cr, Mo or Mo alloy and an upper film of Al or Al alloy.

Claim 12 (Withdrawn): The method of claim 11, further comprising:

removing the upper film before forming the pixel electrode.

Claim 13 (Withdrawn): The method of claim 6, wherein the pixel electrode comprises IZO.

Claim 14 (Withdrawn): The method of claim 6, wherein the data line and the semiconductor layer is formed using a single photoresist film.

Claim 15 (Previously presented): A thin film transistor array panel comprising:

a gate line formed on an insulating substrate;

a gate insulating layer on the gate line;

a semiconductor layer on the gate insulating layer;

a data line formed on the gate insulating layer and including a source electrode;

a drain electrode formed at least in part on the semiconductor layer;

a passivation layer formed on the data line and the drain electrode and having a first contact hole exposing the drain electrode at least in part and a portion of an upper surface of the gate insulating layer; and

a pixel electrode formed on the passivation layer and contacting the drain electrode and the exposed portion of the gate insulating layer through the first contact hole.

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Claim 16 (Previously presented): The thin film transistor array panel of claim 15, wherein at least one of the gate line, the data line, and the drain electrode comprises a lower film of Cr, Mo, or Mo alloy and an upper film of Al or Al alloy.

Claim 17 (Previously presented): The thin film transistor array panel of claim 15, wherein the gate insulating layer comprises silicon nitride and the passivation layer comprises silicon nitride.

Claim 18 (Previously presented): The thin film transistor array panel of claim 15, wherein the pixel electrode comprises IZO.

Claim 19 (Previously presented): The thin film transistor array panel of claim 15, wherein the passivation layer has second and third contact holes exposing end portions of the gate line and the data line, and the thin film transistor array panel further comprises contact assistants contacting the exposed end portions of the gate line and the data line.

Claim 20 (Previously presented): A thin film transistor array panel comprising:

a gate line formed on an insulating substrate;

a gate insulating layer on the gate line;

a semiconductor layer on the gate insulating layer;

a data line formed on the gate insulating layer and including a source electrode;

a drain electrode formed at least in part on the semiconductor layer;

a passivation layer formed on the data line and the drain electrode and having a first contact hole, wherein a bottom of the contact hole is formed by a portion of an upper surface of the drain electrode and a portion of an upper surface of the passivation layer; and

a pixel electrode formed on the passivation layer and contacting the drain electrode and the exposed portion of the gate insulating layer through the first contact hole.

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Claim 21 (Previously presented): The thin film transistor array panel of claim 20, wherein at least one of the gate line, the data line, and the drain electrode comprises a lower film of Cr, Mo, or Mo alloy and an upper film of Al or Al alloy.

Claim 22 (Previously presented): The thin film transistor array panel of claim 20, wherein the gate insulating layer comprises silicon nitride and the passivation layer comprises silicon nitride.

Claim 23 (Previously presented): The thin film transistor array panel of claim 20, wherein the pixel electrode comprises IZO.

Claim 24 (Previously presented): The thin film transistor array panel of claim 20, wherein the passivation layer has second and third contact holes exposing end portions of the gate line and the data line, and the thin film transistor array panel further comprises contact assistants contacting the exposed end portions of the gate line and the data line.

Claim 25 (Previously presented): A thin film transistor array panel comprising:

a gate line formed on an insulating substrate;

a gate insulating layer on the gate line;

a semiconductor layer on the gate insulating layer;

a data line formed on the gate insulating layer and including a source electrode;

a drain electrode formed at least in part on the semiconductor layer;

a passivation layer formed on the data line and the drain electrode and having a first contact hole exposing the drain electrode at least in part and a portion of the gate insulating layer; and

a pixel electrode formed on the passivation layer and contacting the drain electrode and the exposed portion of the gate insulating layer through the first contact hole, wherein the pixel electrode contacts an upper surface of the gate insulating layer.

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Claim 26 (Previously presented): The thin film transistor array panel of claim 25, wherein at least one of the gate line, the data line, and the drain electrode comprises a lower film of Cr, Mo, or Mo alloy and an upper film of Al or Al alloy.

Claim 27 (Previously presented): The thin film transistor array panel of claim 25, wherein the gate insulating layer comprises silicon nitride and the passivation layer comprises silicon nitride.

Claim 28 (Previously presented): The thin film transistor array panel of claim 25, wherein the pixel electrode comprises IZO.

Claim 29 (Previously presented): The thin film transistor array panel of claim 25, wherein the passivation layer has second and third contact holes exposing end portions of the gate line and the data line, and the thin film transistor array panel further comprises contact assistants contacting the exposed end portions of the gate line and the data line.

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EVIDENCE APPENDIX

None.

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RELATED PROCEEDINGS APPENDIX

None.

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